6.5 A 0.65-to-1.4nJ/burst 3-to-10GHz UWB Digital TX in 90nm CMOS for IEEE 802.15.4a

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Recently, the IEEE 802.15.4a standardization committee proposed an alternative physical layer providing ranging on top of low-power low-data-rate communication using UWB as the key technology. The recent draft proposal of the physical layer [1] defines the signal structure depicted in Fig. 6.5.1. An elementary data symbol consists of a burst of concatenated chips present at a given position within the symbol period. This burst is time-hopped within a set of slots inside the symbol period. The chips within the burst are BPSK modulated and upconverted according to the frequency band plan (Fig. 6.5.1). All necessary frequencies are derived as integer multiples of a frequency reference (31.2MHz).

The transmitter (Fig. 6.5.2) is designed according to this standard. Ultra-low power is obtained by switching off the entire TX between each burst. It consists of a digitally controlled oscillator (DCO), a programmable divider (DIV), a digital modulator (DMO), and an early-late detector for DCO frequency calibration. The correct RF frequency is not generated by a traditional PLL, since the large start-up time would drastically reduce the low power advantages of low-duty-cycle communication. Instead, a phase-aligned frequency-locked loop is implemented. Phase alignment is done by forcing the startup process of the DCO to be uniform when it is switched on at each burst. Thereby, the DCO is realigned to the reference clock at each reactivation. This technique does not only have the advantage of substantially reducing the startup time but also truncates the accumulative jitter process. Since the initial phase of the DCO is uniform for each burst, only the frequency needs to be adjusted. This is done using an early-late (fast-slow) detection mechanism operating on each transmitted burst. The DIV produces the chip rate used to clock the burst code register that feeds the DMO. The DMO modulates the RF output of the DCO according to the burst code sequence and the data value.

The 3-to-10GHz frequency range is covered by a single digitally controlled ring oscillator (Fig. 6.5.3). To avoid degrading the SNR of the TX/RX link, the phase of each transmitted chip should be accurate within 15ps at 10GHz which sets the requirement on the jitter of the oscillator and implies a frequency accuracy of 4MHz. The frequency accuracy and 3-to-10GHz frequency range results in the need for 3 different methods to control the DCO. Implementing the full tuning range with a switchable biasing current would entail matching with large transistors for the smallest frequency steps whose capacitances would unbearably slow down the start-up. Therefore, a 6b current source is used for coarse tuning such as to benefit from its power scalability. For the medium tuning, a 5b capacitor bank is used since it does not degrade the start-up time. However, it is limited in the minimum frequency steps by parasitic capacitances. Therefore, the finest tuning is implemented with an 8b tuning on the degeneration resistor of the biasing current mirror. A 4b binary 4b thermometer segmentation is used to ensure a monotonous frequency tuning curve (Fig. 6.5.3). In conclusion, although 13 bits would ideally be sufficient to cover the full band, the necessary overlap between the various frequency tunings lead to 19 control bits. The maximum settling time is below 2ns to achieve 4MHz accuracy, which is less than 10% of the burst time. Transistors to supply and ground on the oscillating nodes ensure a predefined initial state. At TX activation these transistors are released at a reference clock edge guaranteeing fast and uniform startup.

The frequency divider, shown in Fig. 6.5.4, divides the 3-to-10GHz DCO frequency by an integer value from 7 to 20 to produce the chip rate. The fully dynamic divider is realized in true single-phase clock (TSPC) logic based on the work of [2]. It consists of a cascade of 18 half-transparent latches (HTLs) in a loop closed by a precharge unit and clocked by the RF signal. To achieve 10GHz speed, the HTL Clk/Bypass unit has been modified (circuit of Fig. 6.5.4). Any integer division value between 7 and 20 can be obtained by setting the appropriate number of HTLs in bypass mode.

To produce a burst of BPSK modulated chips, the RF LO must be modulated by a +1/–1 code sequence defined in the standard. Modulation is realized by inverting and shaping the carrier at each code transition. A nice feature of the synchronous divider is the fact that the timing required to shape the pulses is available in its intermediate phases (Fig. 6.5.4). Four discrete steps are taken to invert the carrier by using 4 parallel multipliers consecutively activated by properly chosen phases of the divider HTL chain. Each unit multiplies the RF LO with the code value. Thereby, a code transition produces at the sum output an RF LO inversion in 4 discrete steps as a result of the sequential activation of the multipliers.

The DCO RF frequency is calibrated to the desired band prior to transmission by using an early-late detector (ELD). The ELD measures the time difference between a burst duration measured at the divide-by-16 output and a reference clock period. It then generates a 1b value specifying whether the RF frequency is too high or too low. The result is used to increase/decrease the control word setting of the DCO frequency via an external FPGA. Three binary-search calibrations are done to set the coarse, medium, and fine tuning word, after which the RF frequency is within less than 4MHz of the desired one. Drift of the DCO frequency during operation is monitored by the ELD status at every transmitted burst and the DCO control word is adjusted for the next burst.

The TX is realized in a 90nm digital CMOS process with the chip micrograph shown in Fig. 6.5.7. The measured output power is –10dBm with reference to 50Ω. The power consumption of the transmitter from 1V supply is 0.65nJ per 16 chips burst (40pJ/pulse) at 3.5GHz and 1.4nJ/burst (87pJ/pulse) at 10GHz which outperforms state-of-the-art low-power narrowband transmitter implementations [3,4]. For the mandatory mode, this corresponds to 0.65mW to 1.4mW for 1Mb/s data rate with 75% in the DCO and LO distribution, 5% for the DIV, and 20% for the DMO. A transmitted burst is measured on a high bandwidth scope (Fig. 6.5.5). The output spectrum fitting the transmit mask is also shown in the figure. The TX can operate in any 499.2MHz band of the IEEE 802.15.4a. The jitter evolution over a burst is shown in Fig. 6.5.6 and the total accumulated jitter is below $6ps_{rms}$ for the 10GHz carrier where the highest SNR degradation is observed. A $6ps_{rms}$ jitter at 10GHz degrades SNR by less than 1dB for a 1e–4 BER. This implementation demonstrates a low-power UWB TX compatible with the IEEE 802.15.4a draft standard. It proves that for transmission the standard leads to implementations with power consumptions meeting sensor networks requirements.

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[1] IEEE 802.15.4 WPAN Low Data Rate Alternative PHY Layer: http://www.ieee802.org/15/pub/TG4a.html.
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[4] W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe and D. Eggert, “A Fully Integrated 2.4GHz IEEE 802.15.4 Compliant Transceiver for ZigBee Applications,” *ISSCC Dig. Tech. Papers*, pp. 372-373, Feb., 2006.

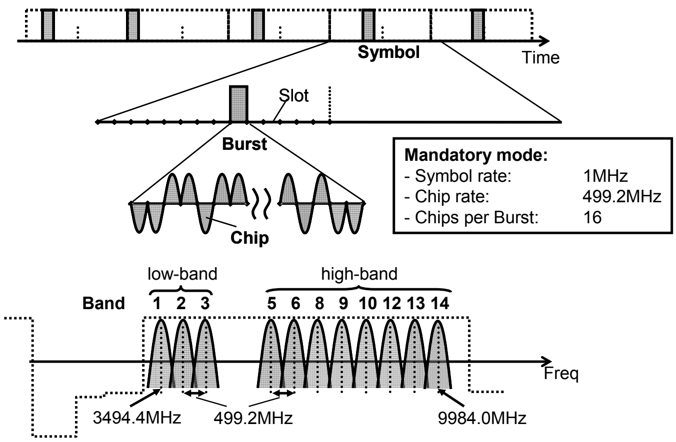

Figure 6.5.1: 802.15.4a standard air interface. Bands 4,7,11 and15 (not shown) are optional and have a different bandwidth. Bands 3 and 9 are mandatory.

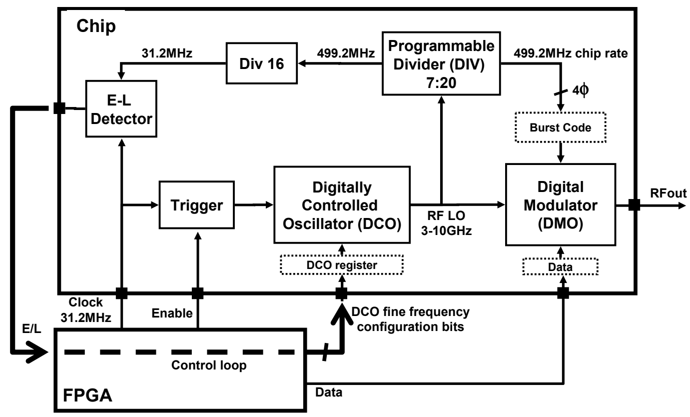

Figure 6.5.2: Architecture of the UWB Transmitter.

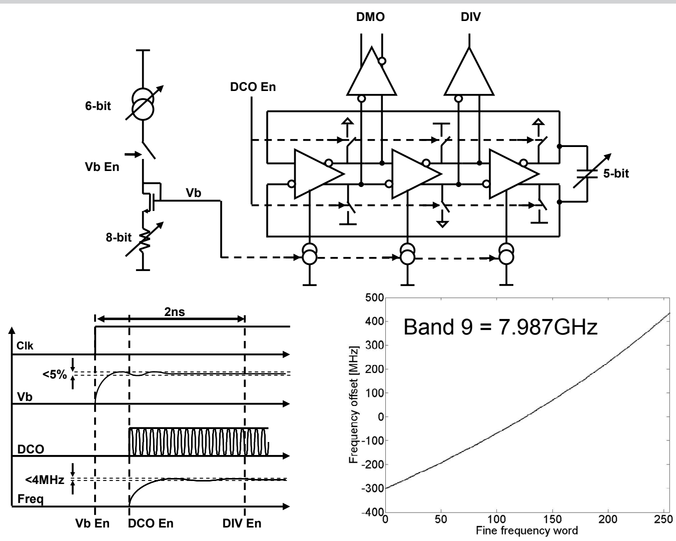

Figure 6.5.3: Block diagram of the DCO with its startup sequenceand measured fine frequency tuning curve around mandatory band 9 (bottom right).

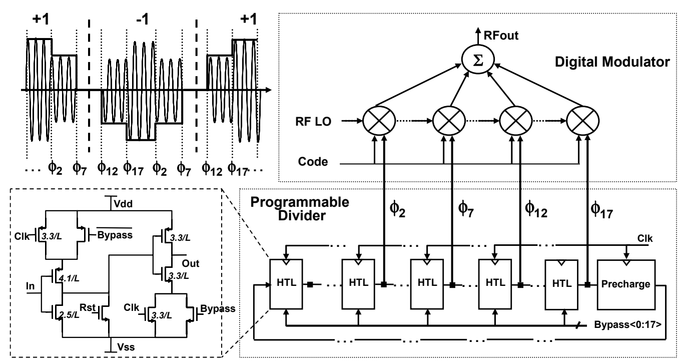

Figure 6.5.4: Programmable divider and modulator architecture.

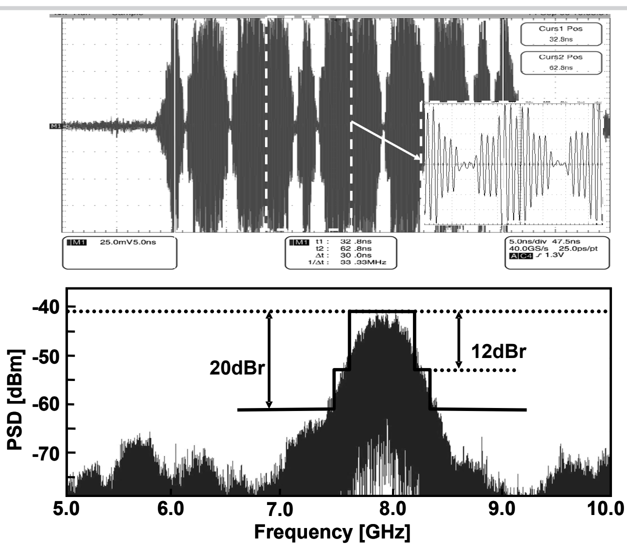

Figure 6.5.5: Time-domain measurement (top) of a single burst and output spectrum (bottom) of a burst stream with pseudo-random code sequence.

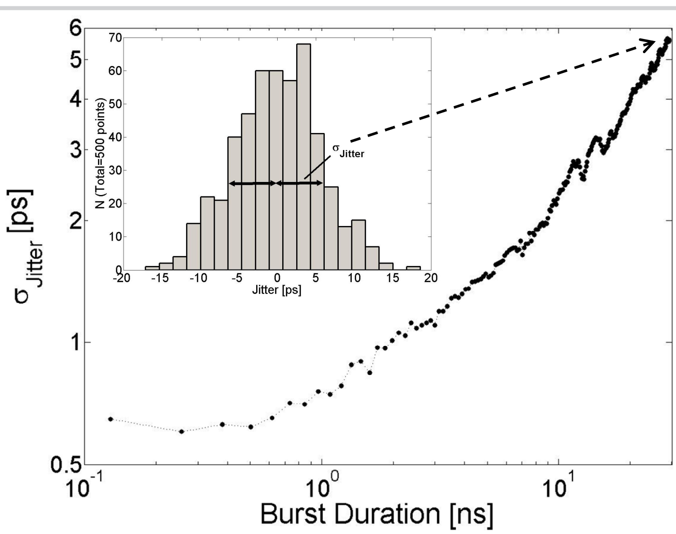

Figure 6.5.6: Measurement of the jitter accumulation along a burst at 10GHz. The histogram of the total accumulated jitter is also shown.

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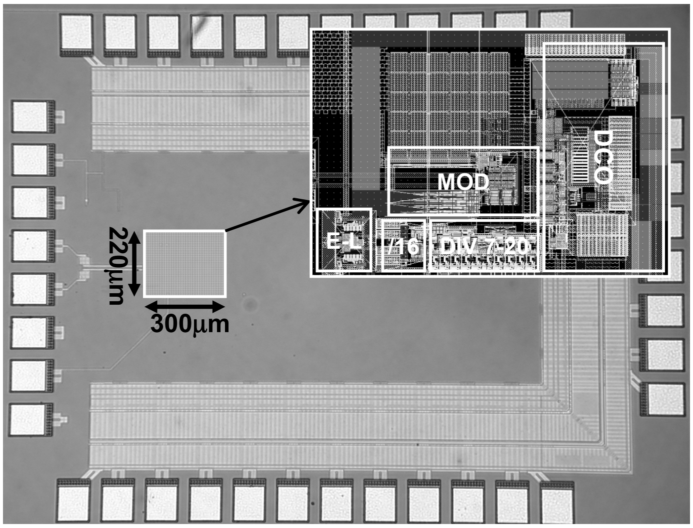

Figure 6.5.7: Chip micrograph (chip area is 1×1.4mm²).

